Assignment 4
Due: Tuesday, December 3, 2013

- **Show all your work clearly and legibly for all your answers.**
- You are required to answer all 8 questions.
- The assignment (written or printed) must be stapled before handing in.
- You may hand in your assignment
  - to the instructor on due date by end of the class or
  - deposit it on hand-in lockers on 4th floor of the E2 building besides the elevator by 430 pm on the due date
- The numbers under [ ] indicate the marks allocated to each question.

1. [2] Describe the general characteristics of a program that would exhibit very little temporal and spatial locality with regard to data accesses.

2. [10] Consider a series of word address references 1, 4, 8, 5, 20, 17, 19, 56, 9, 11, 4, 43, 5, 6, 9, 17. Assuming a direct-mapped cache with **16 one-word blocks** that are initially empty

a. label each reference in the list as a *hit* or a *miss* and fill the respective row for Tag and Index in Table 1

b. show the final contents of the cache by filling in the Address column in Table 2

Table 1: Hit/Miss table

Reference	Hit or Miss	Tag	index
1			
4			
8			
5			
20			
17			
19			
56			
9			
11			
4			
43			
5			
6			
9			
17			

b) Final contents of the Cache: **Table 2**

Block Number	Address
0	
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	
13	
14	
15	
16	

3. [10] Consider a series of word address references 11, 22, 33, 44, 55, 66, 77, 32, 45, 54, 67, 76. Assuming a direct-mapped cache with **8 two-word blocks** that are initially empty, label each reference in the list as a *hit* or a *miss* and fill the respective row for Binary address, Tag and Index in Table 3

Table 3

Reference	Hit or Miss	Address in Binary	Tag	index
11				
22				
33				
44				
55				
66				
77				
32				
45				
54				
67				
76				

4. [10] Consider a series of word address references 1, 134, 212, 1, 135,213,162, 161, 2, 44, 41, 221. Assuming a direct-mapped cache with **Four 4-word** blocks that are initially empty, label each reference in the list as a *hit* or a *miss* and fill the respective rows for Binary address, Tag and Index in Table 4.

Table 4

Reference	Hit or Miss	Address in Binary	Tag	index
1				
134				
212				
1				
135				
213				
162				
161				
2				
44				
41				
221				

5. **[10]** C1 is a direct-mapped Cache with **16 one-word blocks**. C2 is another direct-mapped Cache with **4 four-word blocks**. Assume that the miss penalty for C1 is 8 clock cycles and the miss penalty for C2 is 11 clock cycles. Also assume that the Caches are initially empty.

a. [3] Find the length of a shortest reference string of word addresses for which C2 has a lower miss rate but spends more cycles on Cache misses than C1. Explain your answer

b. [7] For the reference string 0, 4, 8, 11 find the miss cycles in both caches by creating Table 5 below to show your work.

Table 5

Reference	Hit or Miss		Address in Binary	Cache 1		Cache 2	
	Cache C1	Cache C2		Tag	Index	Tag	Index
0							
4							
8							
11							

6. [10] Using the series of references given in problem 2, show the hits and misses and final cache contents for a two-way set-associative cache with one-word blocks and a *total size* of 16 words. Assume LRU replacement. Use table 6 and 7 below

Table 6

Reference	Hit or Miss	Reference	Hit or Miss
1		9	
4		11	
8		4	
5		43	
20		5	
17		6	
19		9	
56		17	

Table 7

Block Number	Element #1 Address	Element #2 Address
0		
1		
2		
3		
4		
5		
6		
7		

7. [5] Consider a virtual memory system with the following properties:

40-bit virtual byte address
16-KB pages
36-bit physical byte address

What is the total size of the page table for each process on this machine, assuming that the valid, protection, dirty, and use bits take a total of 4 bits and that all the virtual pages are in use? (Assume that disk addresses are not stored in the page table.)

8. [3] If all misses are classified into one of three categories -- compulsory, capacity, or conflict

a. Which misses are likely to be reduced when a program is rewritten so as to require less memory?
b. How about if the clock rate of the machine that the program running on is increased?
c. How about if the associativity of the existing cache is increased?