Assignment 3
Due: Tuesday, November 19, 2013

- **Show all your work clearly and legibly for all your answers.**
- You are required to answer first 9 questions. You may provide your answer to the 10th question, which is not for marking.
- The assignment (written or printed) must be stapled before handing in.
- You may hand in your assignment
  - to the instructor on due date by end of the class or
  - deposit it on hand-in lockers on 4th floor of the E2 building besides the elevator by 430 pm on the due date
- The numbers under [ ] indicate the marks allocated to each question.

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1. [10] A program segment has four instructions and the following table summarizes the time (in picoseconds) required by various components in a processor.

Instruction	Inst. Mem	Reg Read	ALU	Data Mem	Reg Write	Total time
lw	100	50	100	100	50	400
sw	100	50	100	100		350
add	100	50	100		50	300
beq	100	50	100			250

   a. What is the speed up you would expect running the program in a pipelined processor over non-pipelined processor?
   b. If the ALU unit takes double the time (ie 200ps), what is the speedup you would expect running the program in a pipelined processor over a non-pipelined processor?

2. [6] Various stages of the datapath have latencies summarized in the following table.
   a. For this implementation, what is the clock cycle time in a pipelined and non-pipelined processor?
   b. For this implementation, what is the total latency of an "*lw*" (load word) instruction in a pipelined and non-pipelined processor?

c. If we can split one of the stages of the pipelined datapath into two new stages, each with half the latency o the original stage, which stage would you split and what is the new clock cycle time of the processor?

IF	ID	EX	MEM	WB
200	300	100	250	150

3. [10] For the following sequence of instructions
   a. [2] Indicate the dependences and their type (as Read After Write (RAW) or Write After Read (WAR) or Write After Write (WAW))
   b. [4] Assume there is no forwarding in this pipelined processor. Indicate hazards and add NOP instructions to eliminate them.
   c. [4] Assume there is full forwarding. Indicate hazards and add NOP instructions to eliminate them

```
sw $16, -100($6)
lw $4, 8($16)
add $5, $4, $4
```

4. [10]
   a. [4] Assume the clock cycle time is 250ps for an implementation. What is the total execution time of the sequence of instructions in question 3 in a pipelined processor without forwarding?
   b. [4] Assume the clock cycle time is 300ps for an implementation. What is the total execution time of the sequence of instructions in question 3 in a pipelined processor with full forwarding?
   c. [2] What is the speedup or slowdown achieved by adding full forwarding (question 4b) to a pipeline that had no forwarding (question 4a)?

5. [4] Using the Graphical representation (similar to figure 4.52 in slide 24 and figure 4.53 in slide 25 of lec-6c1-pipe3-Oct31) of forwarding, show the forwarding paths needed to executed the following three instructions:

```
add $2, $3, $4
add $4, $5, $6
add $5, $3, $4
```

6. [5] Identify all the data dependencies in the following code. Which dependences are data hazards that will be resolved using forwarding? Represent graphically.

   add $2. $5, $4
   add $4, $2, $5
   sw $5, 100($2)
   add $3, $2, $4

7. [5] Consider executing the following code on the pipelined datapath shown below. At the end of the 5th cycle of the execution, which registers are being read and which registers are written?

   add $2. $3, $4
   add $5, $6, $7
   add $8, $9, $10
   add $11, $12, $13
   add $14, $15, $16

8. [10] Consider a program consisting of 100 ***lw*** instructions (consecutively) in which each instruction is dependent upon the instruction before it.
   a. [5] what would the actual CPI be if the program were run on a 5 stage pipelined processor?
   b. [5] If the slowest component in the pipelined datapath takes 500ps, what is the total time to complete this set of 100 ***lw*** instructions? (Assume that the first ***lw*** instruction completes in 2500ps)

9. [20] Refer to **figure 2** for this question. In this figure the instructions in the various stages of the pipeline are not identified. Your task is
   a. to determine as much as you can about the five instructions in the five pipeline stages.
   b. If you cannot fill in a field of an instruction, state why?

   For some fields Refer to slides 7,8 and 13 in lec-6c1-pipe3-Oct31 to identify the control signal values to identify the instruction. For further help, refer to slides 17 through 21 for an example of flow of a set of instructions along the pipelined datapath.

10. **This question is not for marking**. Refer to figure 1. Instead of passing the RegWrite control signal along the datapath registers, if you send the signal to the

register file right after it was generated at the control unit, discuss what happens? Are you skipping any of the assumptions of the pipelined datapath? Are any of the instructions (prior or later) affected by this change?

Figure 1: Pipelined Datapath with Control (refer this figure as see you see fit for any of the questions)

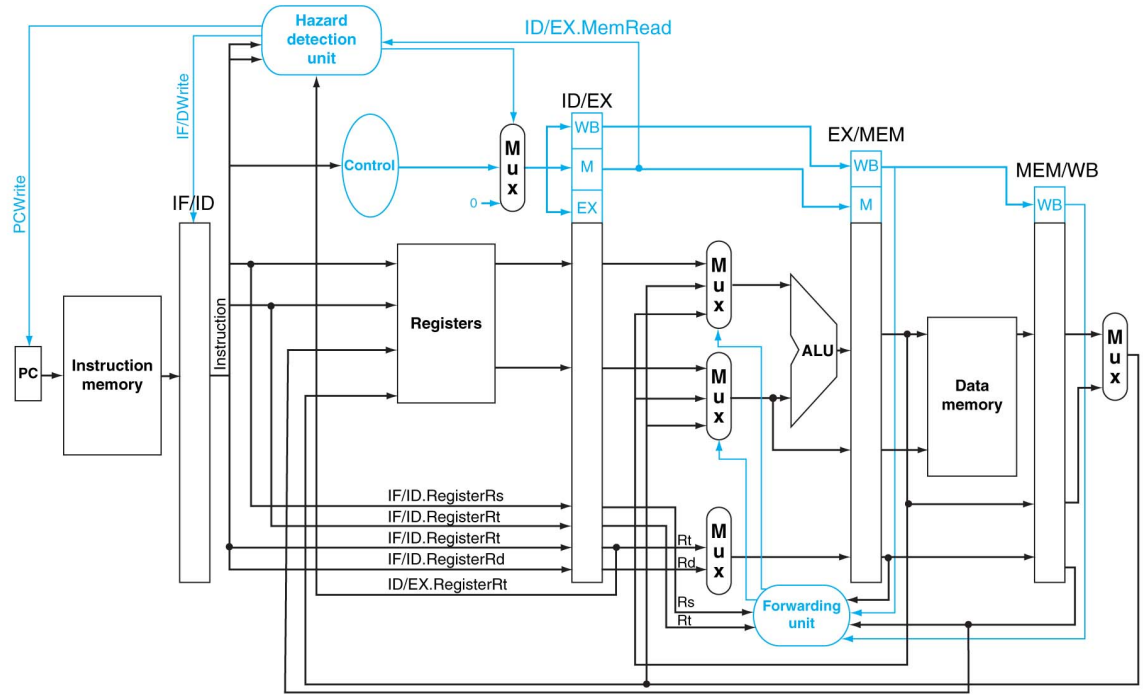

Figure 2: Pipelined datapath with five instructions (not identified)