

1. Solution: $CPI = \text{Sum}(CPI(i) * \text{fraction}(i))$;a. For P1, $CPI = (2+4+6+8+10)/5 = 6.0$ b. For P2, $(3+3+3+3+8)/5 = 4.0$

c.

- CPU Time for P1 = $CPI * IC * \text{clock cycle time} = 6 * (1/3) * 10^{-9}$
= 2 picoseconds;

- Therefore performance of P1 = $(1/2) * 10^9 = 500 * 10^6$

- CPU Time for P2 = $CPI * IC * \text{clock cycle time} = 4.0 * (1/4) * 10^{-9}$
= 1 picoseconds.

- Therefore, Performance of P2 = $(1/1) * 10^9 = 10^9$

- Performance of P2 over performance of P1 = $(1000 * 10^6) / (500 * 10^6) = 2$

2. Solution:

a. Smallest CPI for P1 is 2.

CPU Time = $CPI * IC * \text{clock cycle time} =$ = $2 * (1/3) * 10^{-9} = 0.667 * 10^{-9}$ seconds;**Therefore, peak performance of P1****= $1499.25 \approx 1.5 * 10^9$ instructions/second**

b. Smallest CPI for P1 is 3.

CPU Time = $CPI * IC * \text{clock cycle time} =$ = $3 * (1/4) * 10^{-9} = 0.75 * 10^{-9}$ seconds;**Therefore, peak performance of P2****= $1.333 * 10^9$ instructions/second****3. Solution: 25%** **$10 * 12 + 90 * 4 = 120 + 360 = 480$ cycles;** **$120/480 = 0.25$;****That is, CPU spends 25% of the time doing multiplications.****4. Solution:** Amdahl's law: See page 15 (lec-2D-perf-spe1713) in the lecture notes.**5. Solution:**

a. [2] shift logic left by 3 bits in the value of the register \$s0 and store it in register \$t2

b. [1] R format

c. [2] It is multiplying the content of \$s0 by 2^3 and storing in register \$t2**6. Solution:**

sll \$s1, \$s0, 2

add \$s1, \$s0, \$s1

7.

Instruction	Control Signals						
	RegDst	ALUSrc	Mem2Reg	RegWrite	MemRead	MemWrite	Branch
sub	1	0	0	1	0	0	0
beq	X	0	X	0	0	0	1
or	1	0	0	1	0	0	0
lw	0	1	1	1	1	0	0

Table 3: Control values for a single cycle implementation of MIPS instruction

8.

Solution:

- a. R- Format
- b. No
- c. No
- d. Register 1 (rs) and Register 2 (rt)
- e. Register rd; bits [15-11]
- f. 1001000
- g. No.

9.

Solution:

- a. AND passes through: I-Mem, Regs, ALUSrc Mux, ALU, M2R Mux, RegDst Mux and Reg
= 250+140+70+140+70+70+140=880ps.
- b. add \$t0, \$s1, \$s2