Lab 2: Design and Simulation of Sequential Logic Circuits - Synchronous Counters -

CEG 2136[B] - Computer Architecture I

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School of Electrical Engineering and Computer Science
University of Ottawa

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Introduction

Objectives/Problem

The purpose of the lab is to allow students to practice the conversion of function requirements into logic circuits and introducing students to the design of sequential circuits on the Quartus development environment and the implementation with an FPGA on an oscilloscope.

Solution

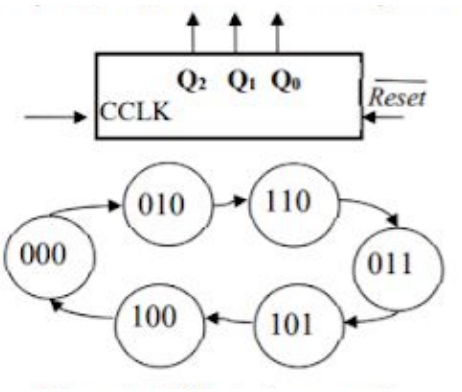
The lab required us to design and complete the circuit for a 3 bit synchronous modulo 6 counter, as illustrated by diagram 2.1.1 in the following section.

To do so, the group broke down the excitation table into simplified boolean expressions for each flip flop, exported the result as a symbol of its own, and utilised it in the final synchronous counter to be shown below.

Design

Diagrams

The provided diagrams are as follows:



Present State	Next State	Synchronous Inputs		
msb lsb $Q_2Q_1Q_0$	msb lsb $Q_2Q_1Q_0$	msb J_2K_2	J_1K_1	lsb J_0K_0
000	010	0 x	1 x	0 x
001	xxx	x x	x x	x x
010	110	1 x	x 0	0 x
011	101	1 x	x 1	x 0
100	000	x 1	0 x	0 x
101	100	x 0	0 x	x 1
110	011	x 1	x 0	1 x
111	xxx	x x	x x	x x

Figure 2.1.1: The excitation table, block diagram, and state diagram of the counter

These were used to determine the kmaps and the corresponding input/output values of all the JK and Q values of the flip flops, as well as of the circuit as a whole, which was then implemented into the circuit pictured in figure 2.3.1.

Components

- Altera Quartus Design Software
- Altera DE2-115 board
    - USB-Blaster cable
    - Power supply 12V/2A
- Coaxial cable
- Wires
- Ribbon Cable

- Probe (unused)
- Oscilloscope

Implementation

Using the provided Altera software to build the circuit, we used three JK flip flops, arranged as illustrated below:

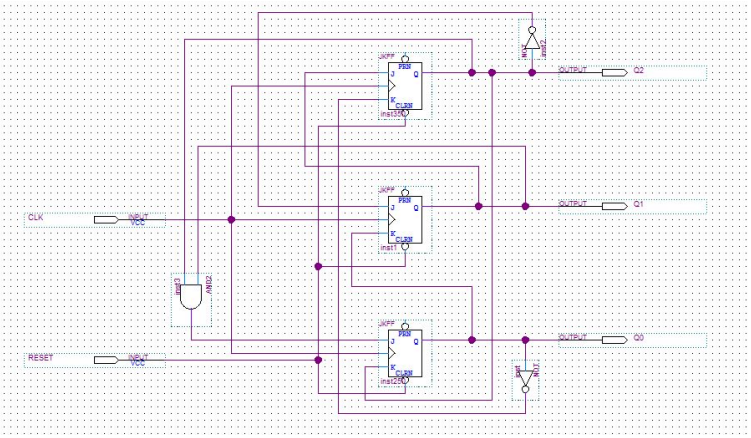


Figure 2.3.1 The Circuit Diagram for the counter

This diagram was first tested to verify outputs, with results shown in the waveform diagram below:

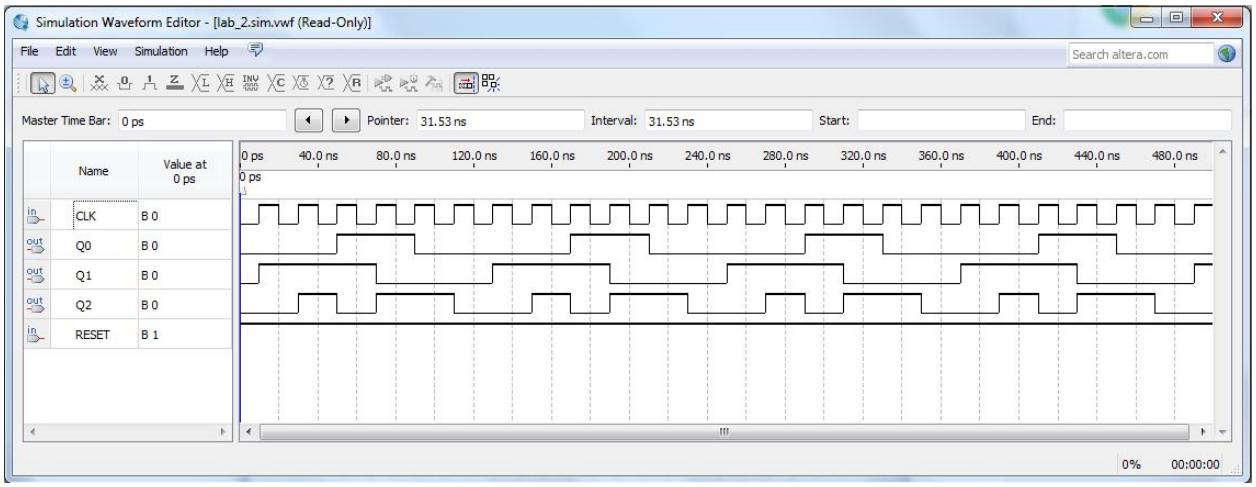


Figure 2.3.2: Waveform diagram for expected output of the circuit

This counter diagram was then exported as a symbol to be used in pin assignments, pictured below:

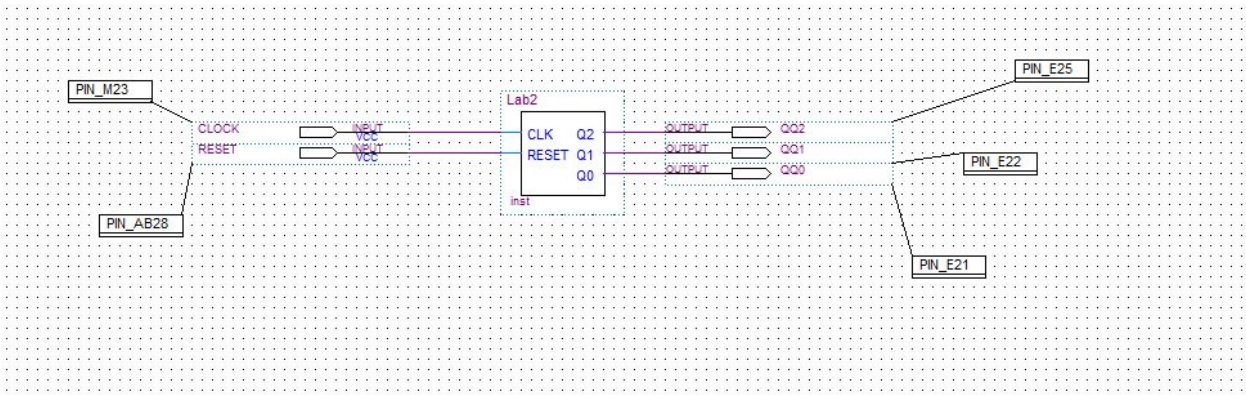


Figure 2.3.3: The pin assignments used in the manual control testing method

This diagram was used for the manual control testing method, by using a push-button and LEDs on the Altera board itself. After this was done, a second diagram was made for the automatic testing method, pictured below:

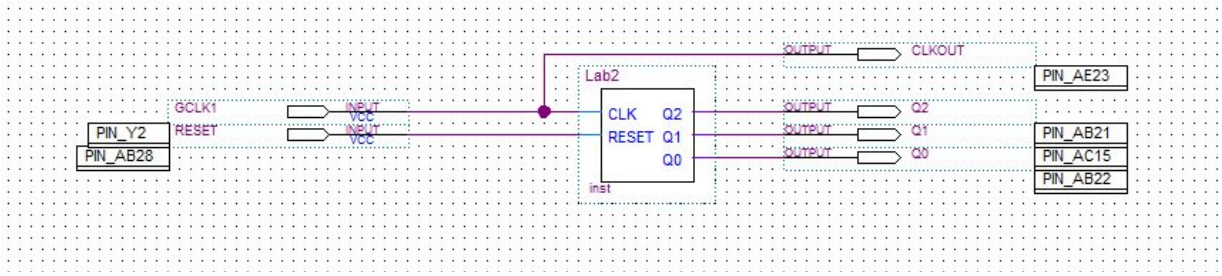


Figure 2.3.4: The pin assignments for the automatic testing method

Once this was completed, it was hooked up to the provided oscilloscope to be tested and verified - which was successfully and quickly done by following the setup instructions on the class brightspace.

Challenges

The lab itself had no large challenges in regards to the complexity or scale of the tasks, however one challenge that occurred was encountered when our code would be unable to run for the testing stage. This was later rectified, as it simply was caused by defective boards that were not working properly.

Verification

Despite the mishaps that occurred along the way, the lab was properly verified without incident - as all our k-maps and circuit diagrams were correct. The outputs are pictured below:

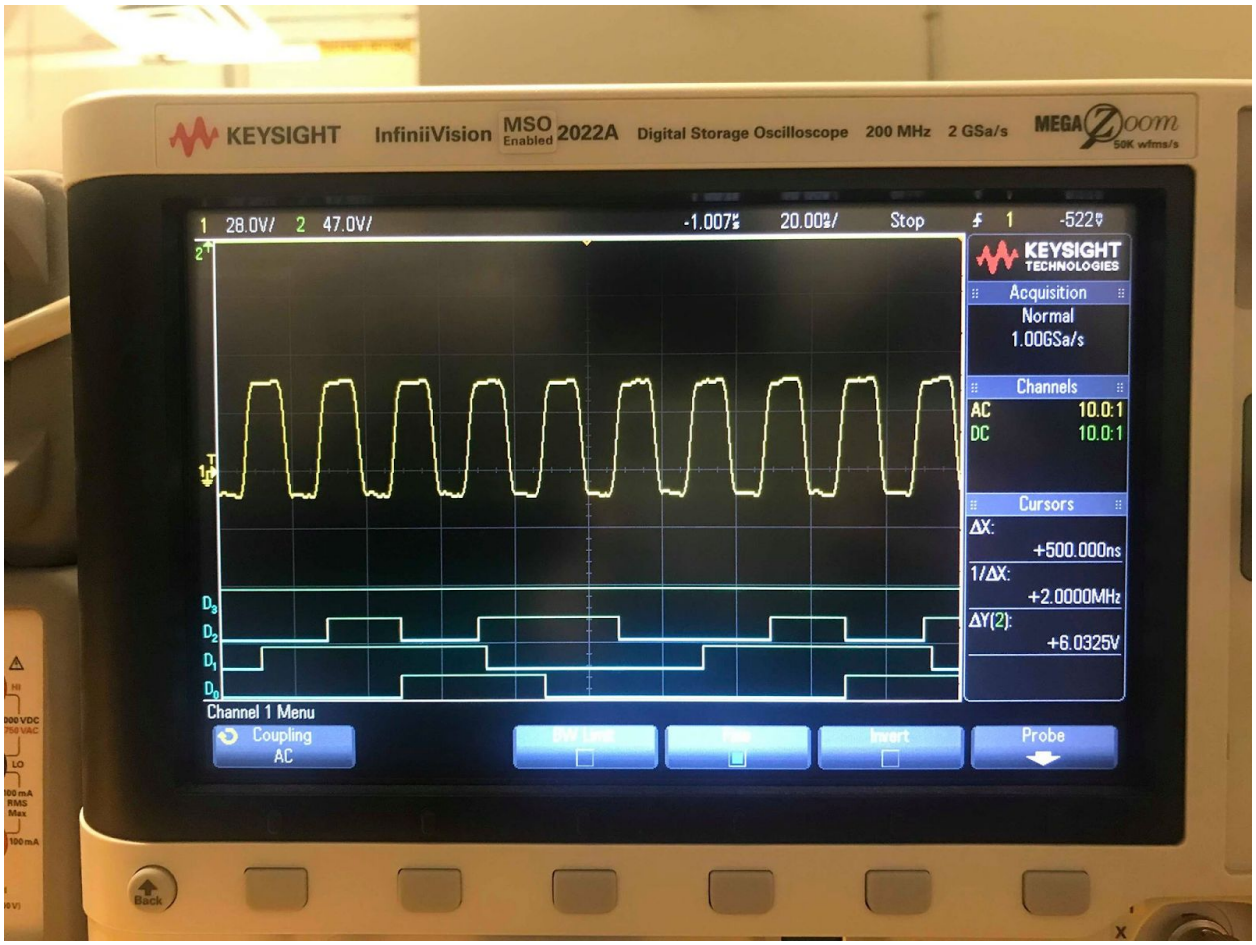
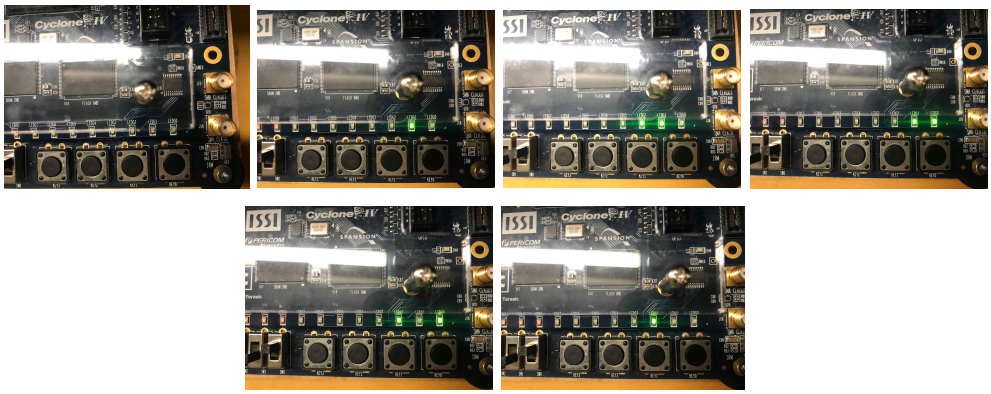


Figure 3.1.1 The oscilloscope showing the successful test results



Figures 3.1.2-7 The various stages shown on the Altera board illustrating the counter following the proper outputs

This made for a smooth lab experience, and easily verified results.

Discussion and Conclusions

Due to the accuracy and the ease of completion of the lab and its information, this lab was a success for our group as this demonstrated a strong understanding of the lab and proper though processes when solving the issues brought up in the lab. Therefore, a reasonable conclusion is that the lab was a success.