UNIVERSITY OF TORONTO

Solutions

Winter 2019 Midterm

Solutions

CSC258: Computer Organization

Duration: 2 hours

February 25th, 2019

Last Name: _____

First Name: _____

Student Number: _____

Lecture section: **L0101 – MWF 1pm**
L0201 – MWF 2pm
L5101 – M 6pm

1 mark each for circling your lecture section and writing your name on the last page.

Instructions:

- **Write your name on the back of this exam paper.**
- **Do not open this exam until you hear the signal to start.**
- Have your student ID on your desk.
- No aids permitted other than writing tools. If you write in pencil, we reserve the right to deny any remark requests.
- Keep all bags and notes far from your desk before the exam begins.
- There are 5 parts on 14 pages. When you hear the signal to start, make sure that your exam is complete before you begin.
- Read over the entire exam before starting.
- If you use any space for rough work or have to user the overflow page, clearly indicate the section(s) that you want marked.

Mark Breakdown

Front/Back:	**/ 2**
Part A:	**/ 47**
Part B:	**/ 28**
Part C:	**/ 28**
Part D:	**/ 15**
Part E:	**/ 10**
Bonus:	**/ 1**

Total: / 128

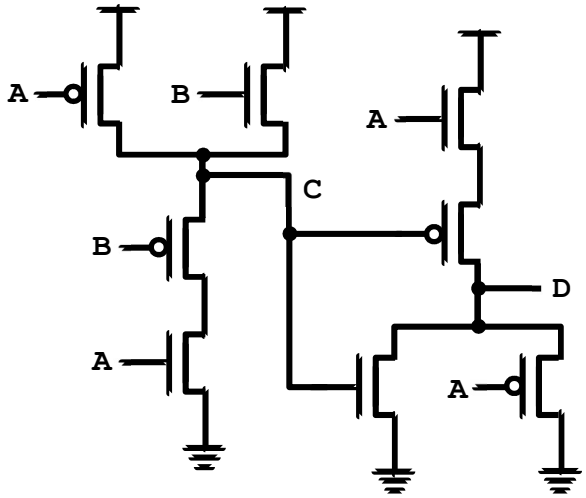
Part A: Short Answer (47 marks)

Answer the following questions in the space provided. When providing a written answer, write **as clearly and legibly as possible**. Marks will not be awarded to unreadable answers.

1. Based on the transistor diagram below, write the most reduced values for C and D in the spaces provided, as a logical expressions of A and B. **(3 marks)**

C = $\overline{A} + B$

D = $A\overline{B}$



2. True or False? Voltage is the measure of electrical potential between two points. **(1 mark)**

True False

3. Doping a semiconductor can involve the addition of what elements? Circle all that apply. **(2 marks)**

   a. **Germanium**
   b. **Boron**
   c. **Oxide**
   d. **Phosphorus**

4. When high voltage is applied to the source and the gate of a MOSFET, current flows between which points? Circle all that apply. **(2 marks)**

   a. **the gate and the source**
   b. **the source and the drain**
   c. **the drain and the gate**
   d. **no current flows between any of these points**

5. Fill in the blank. Drift current results from electrons traveling to the _____ region of a pn junction. **(1 mark)**

n-type (or just n)

6. Given the Karnaugh map on the right, fill in the blanks below with the AND & OR gate costs needed to implement the most reduced form of this circuit. **(2 marks)**

Gate Cost: 3

Gate Cost (including NOTs) = 5

AB \ CD	00	01	11	10
00	0	0	1	1
01	1	1	0	0
11	1	1	0	0
10	0	0	1	1

7. What is the minimal number of flip-flops needed for the 1 second Rate Divider from Lab 5? **(1 mark)**

26

8. Which of the following gates has a low output when all of the input(s) are high? Circle all that apply. **(2 marks)**

a. NAND
b. NOR
c. NOT
d. XOR

(okay if this is not circled, i.e. 3-input XOR case)

9. If a circuit has 4 inputs called A, B, C and D, which of the following are valid maxterms? Circle all that apply. **(2 marks)**

a. A+B+C+D
b. B+A+D+D
c. A+B+C
d. D+A+C+B

10. What is the Boolean expression for a "P > Q" comparator circuit that compares two-bit values P_1P_0 and Q_1Q_0 (where P_1 and Q_1 are the most significant digits)? **(2 marks)**

(could also accept x_1 for this last term)

$$GT = P_1\overline{Q_1} + P_0\overline{Q_0}\,(\overline{P_1}\,\overline{Q_1} + P_1Q_1)$$

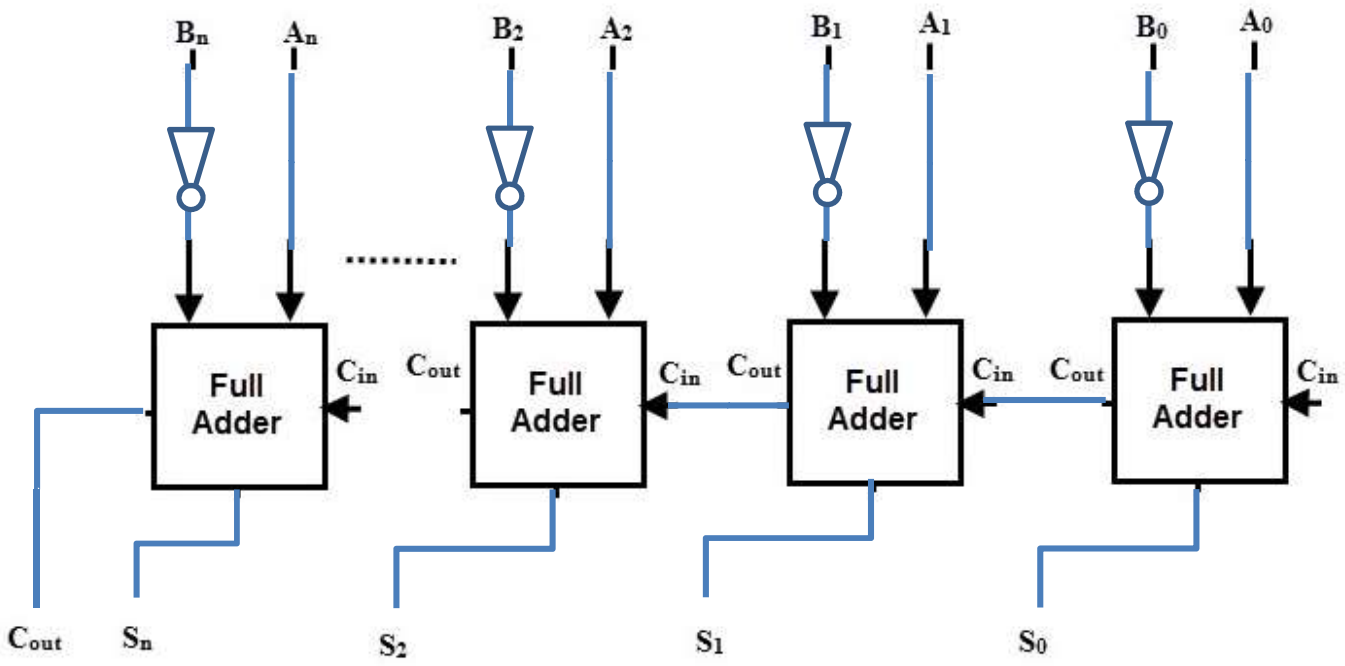
11. True or False: Half of the input cases that a comparator circuit needs to handle are the cases where both inputs are equal. **(1 mark)**

True **False**

12. True or False? If a counter is created using 6 flip flops then the maximum value that the counter can count to is 128. **(1 mark)**

True **False**

13. Complete the following diagram to create a 4-bit binary subtractor, where `S = A - B`. **(4 marks)**



14. If `HEX2[0:6]` is assigned the value `0000110`, what alphanumeric character is displayed? **(1 mark)**

3

15. Convert the following decimal numbers into 8-bit signed binary representation. **(2 marks)**

84 01010100

-64 11000000

16. What are the decimal values of the following 8-bit signed binary numbers? **(2 marks)**

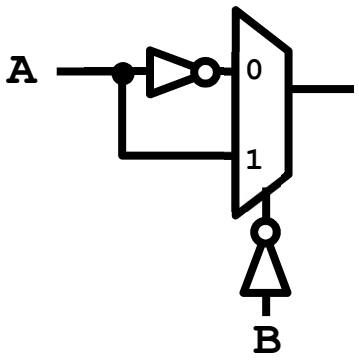
11010110 -42

01111110 126

17. What is the hexadecimal value of the decimal number 693? **(2 marks)**

0x2B5

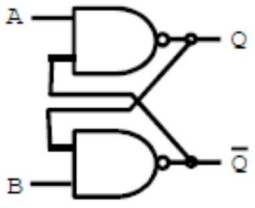
18. What gate is equivalent to the mux circuit on the right? **(1 mark)**



XOR gate

19. Given the latch circuit below, list all the values of A and B that could cause Q to be high. **(3 marks)**

A: 0 B: 0
A: 0 B: 1
A: 1 B: 1 *(if Q was high right before)*



20. When implementing latches and flip-flops in Verilog, what keyword(s) are in the sensitivity list of the `always` block for a flip-flop but not a latch? **(2 marks)**

posedge or negedge

21. Circle the statement below that can be said about register inputs `load_n` and `reset_n`. **(1 mark)**

a. The "`n`" indicates that these inputs are active-low.

b. The "`n`" indicates that these signals apply to all `n` bits of the register.

c. The "`n`" indicates that these inputs are negative edge triggered.

d. The "`n`" has no particular meaning.

22. True or False? Ripple adders and ripple counters are both asynchronous circuits. **(1 mark)**

True False

23. When updating a D flip-flop's value, the new value needs to be on the D input for a period of time before the clock goes high. This new value also needs to stay on the D input for a period of time after the clock goes high. What are the names of these two time delays? **(2 marks)**

Setup time _____ Hold time _____

24. Fill in the blank in the Modelsim command below to create the waveform on the right. **(2 marks)**

```
force clk 0 0, 1 15 -repeat 30
```

25. How many NOT gates are stored on one of the 74LS04 chips used in the lab? **(1 mark)**

6

26. How many AND gates are stored on one of the 74LS32 chips used in the lab? **(1 mark)**

0 *(this chip stores OR gates)*

27. What is significant about pins 7 and 14 on the TTL chips used in the labs? **(2 marks)**

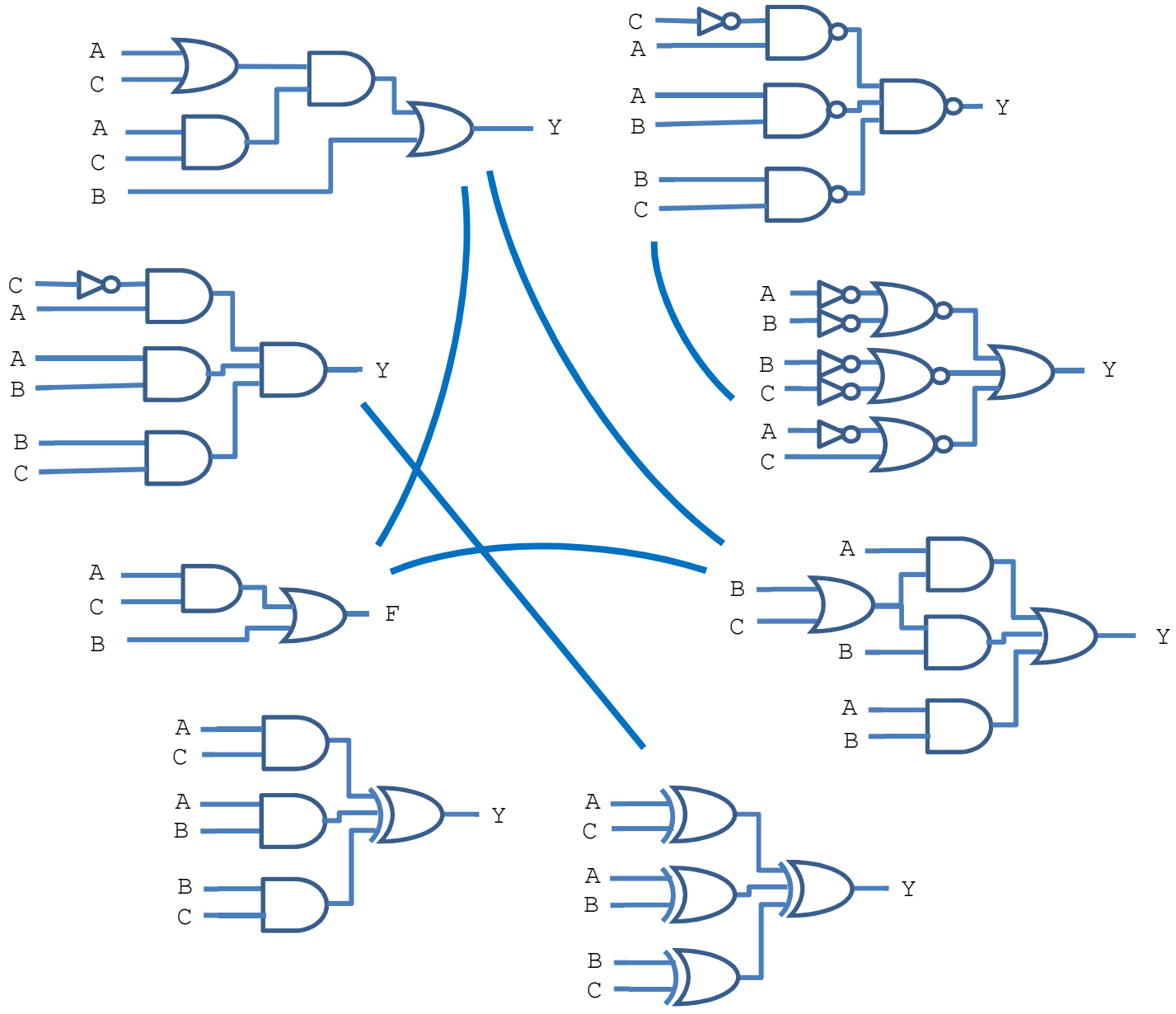
Pin 7: Ground (or 0V)

Pin 14: V_{cc} (or 5V)

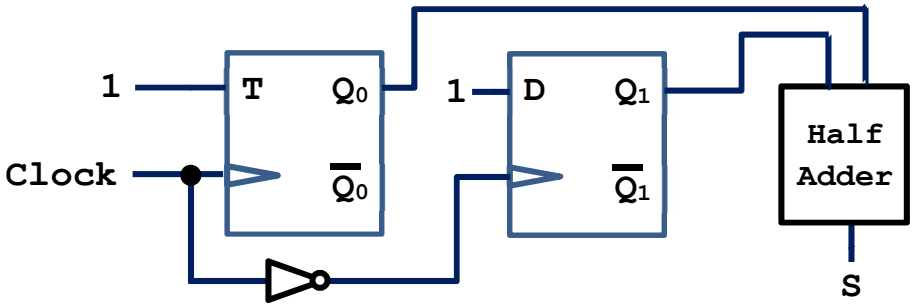
Part B: Slightly Longer Answer (28 marks)

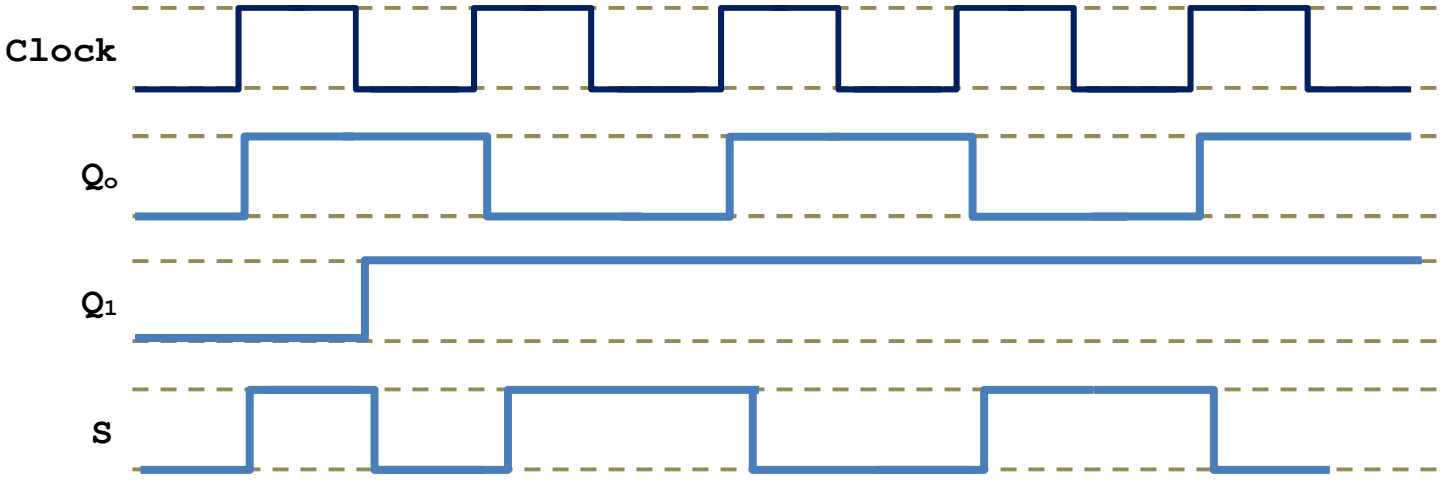
Answer the following questions in the space provided. The final answer is all that is necessary, but showing your work might help if your final answer isn't correct. Again, make sure to write legibly here.

1. Consider the combinational circuits below. Indicate which circuits have the same output behaviour by drawing lines to connect equivalent circuits. **(16 marks)**

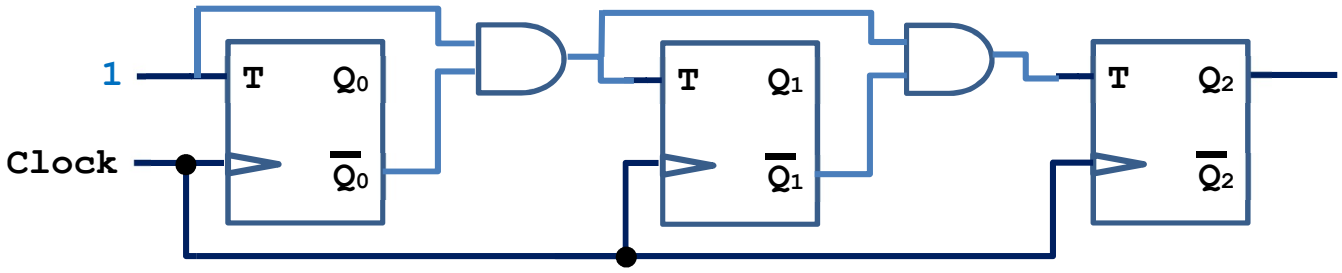


2. For the sequential circuit below, fill in the waveform behaviour for the outputs Q_0, Q_1 and S. Assume the flip-flop output values are all low before the first positive clock edge, and that delays should be factored in your answer. **(6 marks)**





3. Consider the T flip-flops shown below, where Q_0 is the least significant bit and Q_2 is the most significant bit. Complete the diagram to create a **synchronous counter** that counts down instead of up. For full marks, implement this using **no more than two gates**. **(6 marks)**



Part C: Circuit Design and Analysis (28 marks)

Y	$\overline{C}\,\overline{D}$	$\overline{C}\,D$	$C\,D$	$C\,\overline{D}$
$\overline{A}\,\overline{B}$	1	1	0	1
$\overline{A}\,B$	0	1	0	0
$A\,B$	0	X	X	X
$A\,\overline{B}$	1	0	1	1

Consider the Karnaugh map shown above.

1. Fill in the truth table on the right, given the Karnaugh map values above. **(4 marks)**

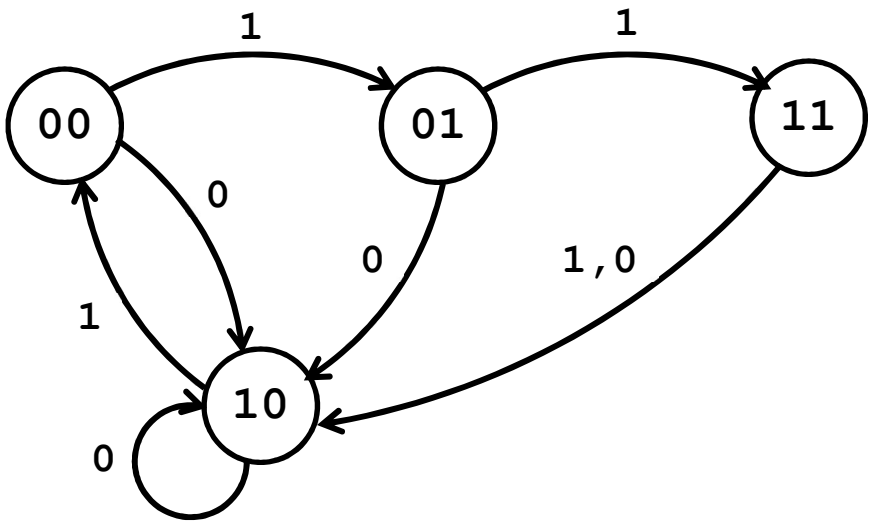
2. On the Karnaugh map above, draw the minterm groupings that would result in the most optimized circuit possible. **(6 marks)**

3. In the space below, write the Boolean equation for the optimized groupings that you made in part 2. **(6 marks)**

Y = $\overline{B}\,\overline{D} + \overline{A}\,\overline{C}D + AC$

A	B	C	D	Y
0	0	0	0	**1**
0	0	0	1	**1**
0	0	1	0	**1**
0	0	1	1	**0**
0	1	0	0	**0**
0	1	0	1	**1**
0	1	1	0	**0**
0	1	1	1	**0**
1	0	0	0	**1**
1	0	0	1	**0**
1	0	1	0	**1**
1	0	1	1	**1**
1	1	0	0	**0**
1	1	0	1	**X**
1	1	1	0	**X**
1	1	1	1	**X**

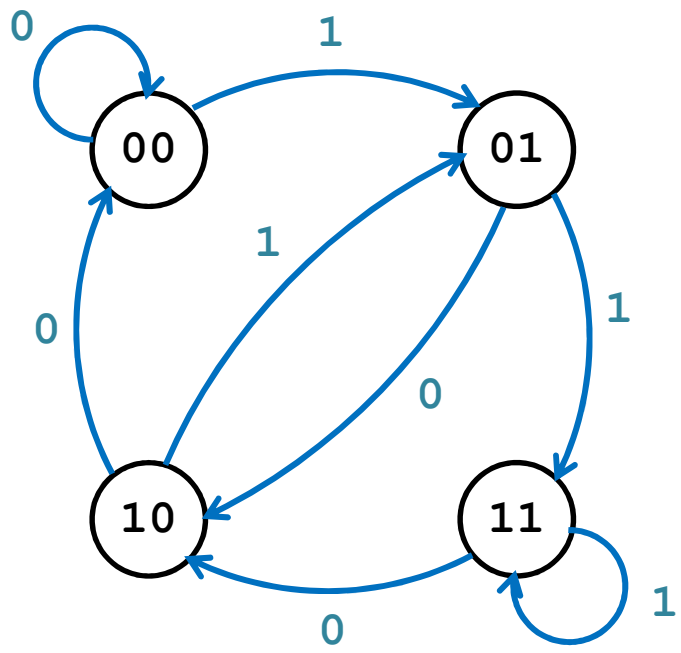
4. Given the finite state diagram below, fill in the truth table diagram on the right with the correct state values. Assume that the numbers in each state below represent F_1 and F_0, respectively. **(8 marks)**



F_1	F_0	X	F_1	F_0
0	0	0	**1**	**0**
0	0	1	**0**	**1**
0	1	0	**1**	**0**
0	1	1	**1**	**1**
1	0	0	**1**	**0**
1	0	1	**0**	**0**
1	1	0	**1**	**0**
1	1	1	**1**	**0**

5. The state diagram below represents flip-flop values in a finite state machine. Draw and label the transitions on this diagram that would make it implement a 2-bit sequence recognizer. **(4 marks)**

   For this question, assume that the recognizer has a single-bit input, and the states below represent the second-last and last input bits seen. For instance, the state `01` indicates that the most recent input was a `1`, and the input immediately before that was a `0`. Make sure to label your transitions!



Part D: Devices (15 marks)

The Verilog modules below implement various devices, as indicated by the module names. Each one has a broken line in the middle (in bold) that needs to be fixed. In the space provided on the right, write a single line of replacement Verilog code to fix the module. **(15 marks)**

```
module shift_reg (Y, D, Clock);
  input D, Clock;
  output reg [7:0] Y = 0;
  always @ (posedge Clock)
     assign Y[7:0] <= Y[6:0];
     Y[7] = D;
endmodule
```

`Y[6:0] = Y[7:1];`

```
module mux (M, A, B, S);
  input A, B, S;
  output M;
  M <= ~SA + SB;
endmodule
```

`assign M = ~S&A + S&B;`

```
module d_latch (Q, D, Clock);
  input D, Clock;
  output reg Q;
  always @ (posedge D)
    if (Clock)
      Q <= D;
endmodule
```

or always @ (*)

`always @ (Clock, D)`

```
module counter (Y, EN, Clock);
  input EN, Clock;
  output reg [3:0] Y = 0;
  always @ (*)
    if (EN)
      Y = Y+1;
endmodule
```

`always @ (posedge Clock)`

```
module full_adder (S, C, X, Y, Z);
  input X, Y, Z;
  output S, C;
  S = X + Y;
endmodule
```

`assign {C,S} = X + Y + Z;`

Part E: Verilog (10 marks)

In the space below, complete the Verilog module for a seven-segment decoder that displays the vowels shown on the right. This module takes in a three-bit code called `V` that indicates what segments in the output `segs` to activate (the display is left blank otherwise).

For full marks, use a `case` statement to implement this module. **(10 marks)**

V	Output
000	"A": 
001	"E": 
010	"I":
011	"O": 
100	"U": 

Note: The 20% rule is in effect on this question. If you don't know how to do this question, write "I don't know" and you will get 2 marks automatically.

```
module seven_seg_vowels (segs, V);
   input [2:0] V;
   output reg [0:6] segs;

   always @ (*)
      case (V)
         3'b000: segs = 7'b0001000;
         3'b001: segs = 7'b0110000;
         3'b010: segs = 7'b1001111;
         3'b011: segs = 7'b0000001;
         3'b100: segs = 7'b1000001;
         default: segs = 7'b1111111;
      endcase

endmodule
```

Bonus Question: ***What are the names of two of the TAs in your lab room? (1 mark)***

_____

The rest of this page is left blank intentionally for answer overflows.

Please enter your first and last name in the space below. Do NOT write your student number here.