Question 1 *(25 points)*

Find a set of minimum sum of products expressions that cover the following system of logic functions using the Quine-McCluskey method.

$F(a,b,c,d) = \sum m(0, 3, 5, 7) + \sum d(13, 14, 15)$

$G(a,b,c,d) = \sum m(0, 5, 6, 7, 8) + \sum d(13, 14, 15)$

Question 2 *(25 points)*

Digital engineer B. I. Nary has just completed the design of a sequential circuit which has the following state table:

Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
S_0	S_5	S_1	0	0
S_1	S_5	S_6	0	0
S_2	S_2	S_6	0	0
S_3	S_0	S_1	1	0
S_4	S_4	S_3	0	0
S_5	S_0	S_1	0	0
S_6	S_5	S_1	1	0

His assistant, F. L. Ipflop, who has just completed this course, claims that his design is fully equivalent to Mr. Nary's circuit. Mr. Ipflop's design has the following state table:

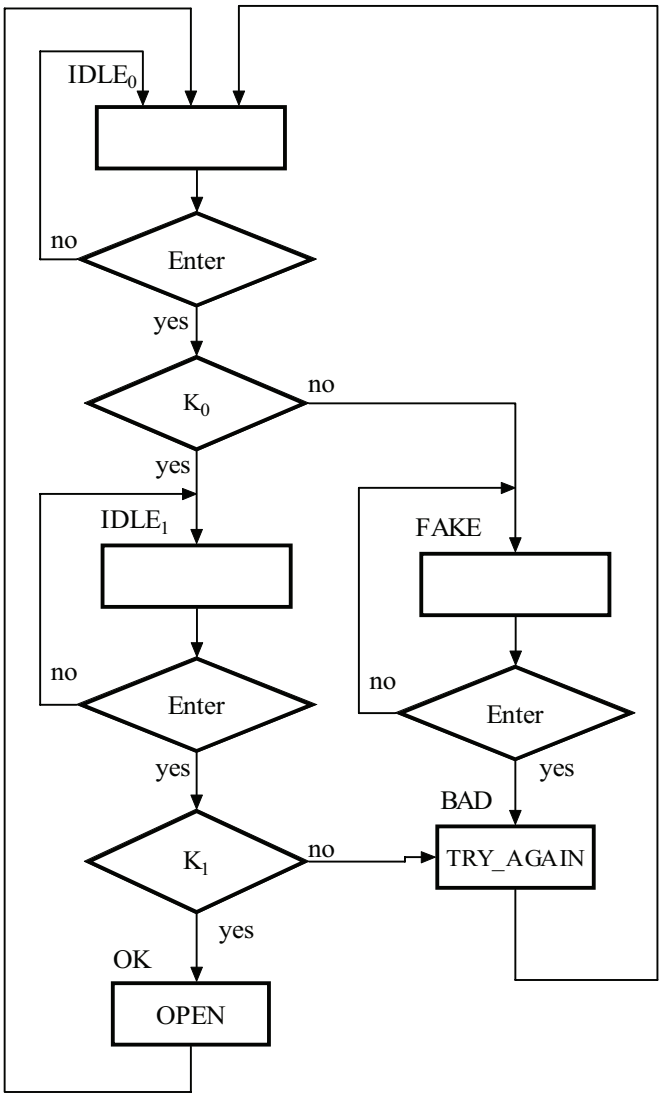
Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	*a*	*b*	0	0
b	*a*	*c*	0	0
c	*a*	*b*	1	0

(a) Is Mr. Ipflop correct? (Prove your answer.)

(b) If Mr. Nary's circuit is always started in state S_0, can be used Mr. Ipflop's design to replace Mr. Nary's circuit? (Prove your answer by showing equivalent states, state diagrams,etc

Question 3 *(25 points)*

Modify the following ASM diagram such that only one input variable is tested in every state.
Draw the modified ASM diagram. Realize this controller using a PROM, multiplexers and a counter-register to implement the *next state* function and the *output* function. Draw the logic diagram of your circuit and give the content of your PROM. Is your controller a Mealy or a Moore FSM?



Question 4 *(25 points)*

A Mealy system with one input *x* and one output *z* produces a 1 output iff *x* has been 1 for three consecutive clock times, like in the sample input/output (*x*/*z*) trace shown bellow:

```
x   0 1 1 0 1 1 1 0 0 1 0 1 1 1 1 1 0 0
z   ? 0 0 0 0 0 1 0 0 0 0 0 0 1 1 1 0 0
```

Show the state diagram of this FSM.